REMARKS

The Office Action dated January 9, 2004, has been received and carefully noted. The following remarks are submitted as a full and complete response thereto. Claims 1-6 are pending in the above-cited application and are respectfully submitted for consideration.

Claims 1 and 2 were again rejected under 35 U.S.C. § 102(a) as being anticipated by *Muller et al.* (U.S. Patent No. 5,909,686 or *Muller '686*). Claims 3-6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Muller '686* in view of *Muller et al.* (U.S. Patent No. 6,119,196 or *Muller '196*). The above rejections are respectfully traversed according to the remarks that follow.

The present invention is directed to, according to claim 1, a network switch stack configuration. The configuration includes a first network switch comprising a plurality of data ports, a first stacking port, and a first CPU interface, a second network switch having a plurality of data ports, a second stacking port, and a second CPU interface and a common CPU connected to the first CPU interface and the second CPU interface. Additionally, the first stacking port and the second stacking port are communicatively connected, such that incoming packets on any of the plurality of data ports on the first and second switches can be effectively switched to any of the plurality of data ports on either of the first and second network switches and the first and second switches add module headers to the incoming packets and the first and second stacking ports read the

module headers to determine egress ports for the packets. Claims 2-6 are dependent upon claim 1.

Muller '686 is directed to a method and apparatus for providing hardware-assisted CPU access to a forwarding database. A switch fabric provides access to a forwarding database on behalf of a processor, and includes a memory access interface configured to arbitrate access to a forwarding database memory. The switch fabric includes interfaces for communicating with a CPU, shared memory, network ports and a cascading interface communicating with one or more switch elements.

Muller '196 is directed to a method and apparatus for managing a buffer memory in a packet switch that is shared between multiple ports in a network system. The apparatus comprises a plurality of slow data port interfaces configured to transmit data at a first data rate between a slow data port and the buffer memory and a plurality of fast data port interfaces configured to transmit data at a second data rate between a fast data port and the buffer memory. A first level arbiter is coupled to the plurality of slow data port interfaces, where the first level arbiter chooses an access request of one the slow data ports and outputs the access request.

In the Office Action, the Office acknowledges that the claims are rejected over new grounds, even though the same patent references are cited against the claims. With respect to the rejection of claim 1, the change from the prior rejection is as follows: "Each of the switch elements 100 in the system shown in figure 1 inherently add to each of the incoming data packets a header for routing the data packets to a destination; and

[to] read the headers to determine egress port[s] according to the information of the headers; col. 13, lines 9-22."

While the Office is correct that the cited section of *Muller '686* details fields of the packet that could be found in a packet header, there is no disclosure of a *module* header. Claim 1 recited, in part, "wherein the first and second switches add *module* headers to the incoming packets." The rejection appears to take the position that a module header is somehow synonymous with a generic header, and Applicants respectfully assert that there is no support for such a position.

The instant specification clearly describes the function and makeup of a module header according to one embodiment of the present invention. Page 100, lines 29-32, discloses that "[t]he module header information, appended to the packet by the source, is received by IPIC 90 from the P channel. The module header includes the module ID bitmap, COS, mirrored-to port/switch information, trunk group ID, etc. The constructed packet is then sent onto the high performance interface 261." A full description of composition of the module header is provided in the specification of the instant application at page 102, line 4 to page 103, line 29. Thus, Applicants respectfully assert that the recitation of module header in claim 1 does not read on a generic header and that *Muller '686* fails to teach or suggest such an element. For at least this reason, Applicants respectfully assert that the anticipation rejection of claim 1 is improper and should be withdrawn.

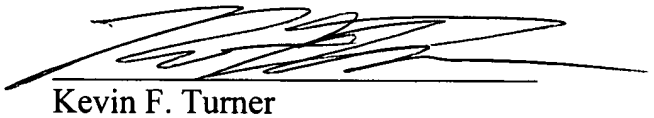
Additionally, Applicants also respectfully traverse the Office's position that a header is inherently added to each incoming packet. While it could conceivably be asserted that *Muller '686* discloses the use of fields of the packet to determine an output port, *Muller '686* fails to teach or suggest *adding* a header to an *incoming* packet. While the rejection appears to allege that such a function would be "inherent," Applicants note that the use of inherent teachings in rejections is not so liberal. "Inherency, however may not be established by probabilities or possibilities. The mere fact that a certain thing *may* result from a given set of circumstances is not sufficient." Continental Can Co. USA Inc. v. Monsanto Co., 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). As such, for this additional reason, Applicants respectfully assert that the anticipation rejection of claim 1 is improper and should be withdrawn.

Thus, Applicants respectfully assert that any rejection of claim 1 over *Muller '686* and/or *Muller '196* would be improper for failing to teach or suggest all of the elements of that claim. On the basis of the above, independent claim 1 is respectfully asserted to be patentable, and as a consequence the dependent claims 2-6 are patentable as well. It is therefore respectfully requested that claims 1-6 be allowed and this application be allowed to pass to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



Kevin F. Turner
Registration No. 43,437

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

KFT:lls